BE(E&TC) DIV-A

VLSI DESIGN & TECHNOLOGY

QUIZ(4 Groups)

1 An Assert is _____ command.
a. Sequential
b. Concurrent
c. Both a and b
d. None of the above

2 The 'next' statements skip the remaining statement in the _____ iteration of loop and execution starts from first statement of next iteration of loop.
a. Previous
b. Next
c. Current (present)
d. None of the above

3 Which among the following wait statement execution causes the enclosing process to suspend and then wait for an event to occur on the signals?
a. Wait until Clk = '1'
b. Wait on x,y,z
c. Wait on clock until answer > 80
d. Wait for 12 ns

4 In composite data type of VHDL, the record type comprises the elements of _____data types.
a. Same
b. Different
c. Both a and b
d. None of the above

5
```
process (a, b) begin
if a = '1' then
w <= b;
end if;
end process;
process (a, c) begin
if a = '0' then
w <= c;
end if;
end process;
```

Ans *unsynth:* single assignment rule — can't have multiple processes driving the same signal

6
```
process begin
wait until rising_edge(a);
w <= not w;
end process;
```

Ans *good:* w=flop // or bad coding style, because state machine without reset

7
```
b <= a;
if b = '1' generate
w <= c;
end generate;
if b = '0' generate
w <= d;
end generate;
```
Ans *illegal:* dynamic test in generate

8
```
process begin
w <= '0';
wait until (a = '0');
p: loop
wait until rising_edge(b);
next p when (a = '1');
w <= c xor d;
end loop;
end process;
```

Ans *unsynth:* different wait conditions

9
```
process (m) begin
for i in 15 downto 0 loop
if 3 >= i then
y(i) <= '0';
else
y(i) <= m(i-3);
end if;
end loop;
end process;
```

Ans *good:* y = comb

10
```
process begin
wait until rising_edge(a);
if b = '1' then
wait until rising_edge(a);
```

```
w <= b;
else
w <= c;
end if;
end process;
```

Ans *good:* w=flop

11 **What is Body effect ?**

Ans The threshold voltage of a MOSFET is affected by the voltage which is applied to the back contact. The voltage difference between the source and the bulk, VBS changes the width of the depletion layer and therefore also the voltage across the oxide due to the change of the charge in the depletion region. This results in a difference in threshold voltage which equals the difference in charge in the depletion region divided by the oxide capacitance, yielding:

12 **What are standard Cell's?**

Ans In semiconductor design, standard cell methodology is a method of designing Application Specific Integrated Circuits (ASICs) with mostly digital-logic features. Standard cell methodology is an example of design abstraction, whereby a low-level VLSI-layout is encapsulated into an abstract logic representation (such as a NAND gate). Cell-based methodology (the general class that standard-cell belongs to) makes it possible for one designer to focus on the high-level (logical function) aspect of digital-design, while another designer focused on the implementation (physical) aspect. Along with semiconductor manufacturing advances, standard cell methodology was responsible for allowing designers to scale ASICs from comparatively simple single-function ICs (of several thousand gates), to complex multi-million gate devices (SoC).

13 **What are Design Rule Check (DRC) and Layout Vs Schematic (LVS) ?**

Ans Design Rule Check (DRC) and Layout Vs Schematic (LVS) are verification processes. Reliable device fabrication at modern deep submicrometre (0.13 μm and below) requires strict observance of transistor spacing, metal layer thickness, and power density rules. DRC exhaustively compares the physical netlist against a set of "foundry design rules" (from the foundry operator), then flags any observed violations. LVS is a process that confirms that the layout has the same structure as the associated schematic; this is typically the final step in the layout process. The LVS tool takes as an input a schematic diagram and the extracted view from a layout. It then generates a netlist from each one and compares them. Nodes, ports, and device sizing are all compared. If they are the same, LVS passes and the designer can continue. Note: LVS tends to consider transistor fingers to be the same as an extra-wide transistor. For example, 4 transistors in parallel (each 1 um wide), a 4-finger 1 um transistor, and a 4 um transistor are all seen as the same by the LVS tool. Functionality of .lib files will be taken from spice models and added as an attribute to the .lib file.

14 **What are steps involved in Semiconductor device fabrication ?**

Ans This is a list of processing techniques that are employed numerous times in a modern electronic device and do not necessarily imply a specific order.

Wafer processing
Wet cleans
Photolithography
Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
Dry etching
Wet etching
Plasma ashing
Thermal treatments
Rapid thermal anneal
Furnace anneals
Thermal oxidation
Chemical vapor deposition (CVD)
Physical vapor deposition (PVD)
Molecular beam epitaxy (MBE)
Electrochemical Deposition (ECD). See Electroplating
Chemical-mechanical planarization (CMP)
Wafer testing (where the electrical performance is verified)
Wafer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card.)
Die preparation
Wafer mounting
Die cutting
IC packaging
Die attachment
IC Bonding
Wire bonding
Flip chip
Tab bonding
IC encapsulation
Baking
Plating
Lasermarking
Trim and form
IC testing

15 **What is Clock distribution network ?**

Ans In a synchronous digital system, the clock signal is used to define a time reference for the movement of data within that system. The clock distribution network distributes the clock signal(s) from a common point to all the elements that need it. Since this function is vital to the operation of a synchronous system, much attention has been given to the characteristics of these clock signals and the electrical networks used in their distribution. Clock signals are often regarded as simple control signals; however, these signals have some very special characteristics and attributes.

Clock signals are typically loaded with the greatest fanout, travel over the greatest distances, and operate at the highest speeds of any signal, either control or data, within the entire synchronous system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Furthermore, these clock signals are particularly affected by technology scaling (see Moore's law), in that long global interconnect lines become significantly more resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the increasing significance of clock distribution on synchronous performance. Finally, the control of any differences and uncertainty in the arrival times of the clock signals can severely limit the maximum performance of the entire system and create catastrophic race conditions in which an incorrect data signal may latch within a register.

The clock distribution network often takes a significant fraction of the power consumed by a chip. Furthermore, significant power can be wasted in transitions within blocks, even when their output is not needed. These observations have lead to a power saving technique called clock gating, which involves adding logic gates to the clock distribution tree, so portions of the tree can be turned off when not needed

16 **What is Netlist ?**

Ans Netlists are connectivity information and provide nothing more than instances, nets, and perhaps some attributes. If they express much more than this, they are usually considered to be a hardware description language such as Verilog, VHDL, or any one of several specific languages designed for input to simulators.

Most netlists either contain or refer to descriptions of the parts or devices used. Each time a part is used in a netlist, this is called an "instance." Thus, each instance has a "master", or "definition". These definitions will usually list the connections that can be made to that kind of device, and some basic properties of that device. These connection points are called "ports" or "pins", among several other names.

An "instance" could be anything from a vacuum cleaner, microwave oven, or light bulb, to a resistor, capacitor, or integrated circuit chip.

Instances have "ports". In the case of a vacuum cleaner, these ports would be the three metal prongs in the plug. Each port has a name, and in continuing the vacuum cleaner example, they might be "Neutral", "Live" and "Ground". Usually, each instance will have a unique name, so that if you have two instances of vacuum cleaners, one might be "vac1" and the other "vac2". Besides their names, they might otherwise be identical.

Nets are the "wires" that connect things together in the circuit. There may or may not be any special attributes associated with the nets in a design, depending on the particular language the netlist is written in, and that language's features.

Instance based netlists usually provide a list of the instances used in a design. Along with each instance, either an ordered list of net names are provided, or a list of pairs provided, of an

instance port name, along with the net name to which that port is connected. In this kind of description, the list of nets can be gathered from the connection lists, and there is no place to associate particular attributes with the nets themselves. SPICE is perhaps the most famous of instance-base.

Net-based netlists usually describe all the instances and their attributes, then describe each net, and say which port they are connected on each instance. This allows for attributes to be associated with nets. EDIF is probably the most famous of the net-based netlists.

17 **What Physical timing closure ?**

Ans Physical timing closure is the process by which an FPGA or a VLSI design with a physical representation is modified to meet its timing requirements. Most of the modifications are handled by EDA tools based on directives given by a designer. The term is also sometimes used as a characteristic, which is ascribed to an EDA tool, when it provides most of the features required in this process. Physical timing closure became more important with submicrometre technologies, as more and more steps of the design flow had to be made timing-aware. Previously only logic synthesis had to satisfy timing requirements. With present deep submicrometre technologies it is unthinkable to perform any of the design steps of placement, clock-tree synthesis and routing without timing constraints. Logic synthesis with these technologies is becoming less important. It is still required, as it provides the initial netlist of gates for the placement step, but the timing requirements do not need to be strictly satisfied any more. When a physical representation of the circuit is available, the modifications required to achieve timing closure are carried out by using more accurate estimations of the delays.

18 **What Physical verification ?**

Ans Physical verification of the design, involves DRC(Design rule check), LVS(Layout versus schematic) Check, XOR Checks, ERC (Electrical Rule Check) and Antenna Checks. XOR Check

This step involves comparing two layout databases/GDS by XOR operation of the layout geometries. This check results a database which has all the mismatching geometries in both the layouts. This check is typically run after a metal spin, where in the re-spin database/GDS is compared with the previously taped out database/GDS. Antenna Check

Antenna checks are used to limit the damage of the thin gate oxide during the manufacturing process due to charge accumulation on the interconnect layers (metal, polysilicon) during certain fabrication steps like Plasma etching, which creates highly ionized matter to etch. The antenna basically is a metal interconnect, i.e., a conductor like polysilicon or metal, that is not electrically connected to silicon or grounded, during the processing steps of the wafer. If the connection to silicon does not exist, charges may build up on the interconnect to the point at which rapid discharge does take place and permanent physical damage results to thin transistor gate oxide. This rapid and destructive phenomenon is known as the antenna effect. The Antenna ratio is defined as the ratio between the physical area of the conductors making up the antenna to the total gate oxide area to which the antenna is electrically connected. ERC (Electrical rule check)

ERC (Electrical rule check) involves checking a design for all well and substrate areas for proper contacts and spacings thereby ensuring correct power and ground connections. ERC steps can also involve checks for unconnected inputs or shorted outputs.

19 **What is Stuck-at fault ?**

Ans A Stuck-at fault is a particular fault model used by fault simulators and Automatic test pattern generation (ATPG) tools to mimic a manufacturing defect within an integrated circuit. Individual signals and pins are assumed to be stuck at Logical '1', '0' and 'X'. For example, an output is tied to a logical 1 state during test generation to assure that a manufacturing defect with that type of behavior can be found with a specific test pattern. Likewise the output could be tied to a logical 0 to model the behavior of a defective circuit that cannot switch its output pin.

20 **What is Different Logic family ?**

Ans Listed here in rough chronological order of introduction along with their usual abbreviations of Logic family

* Diode logic (DL)
* Direct-coupled transistor logic (DCTL)
* Complementary transistor logic (CTL)
* Resistor-transistor logic (RTL)
* Resistor-capacitor transistor logic (RCTL)
* Diode-transistor logic (DTL)
* Emitter coupled logic (ECL) also known as Current-mode logic (CML)
* Transistor-transistor logic (TTL) and variants
* P-type Metal Oxide Semiconductor logic (PMOS)
* N-type Metal Oxide Semiconductor logic (NMOS)
* Complementary Metal-Oxide Semiconductor logic (CMOS)
* Bipolar Complementary Metal-Oxide Semiconductor logic (BiCMOS)
* Integrated Injection Logic (I2L)

21 **What is Different Types of IC packaging ?**

Ans IC are packaged in many types they are:

* BGA1
* BGA2
* Ball grid array
* CPGA
* Ceramic ball grid array
* Cerquad
* DIP-8
* Die attachment
* Dual Flat No Lead
* Dual in-line package
* Flat pack
* Flip chip
* Flip-chip pin grid array
* HVQFN

* LQFP
* Land grid array
* Leadless chip carrier
* Low insertion force
* Micro FCBGA
* Micro Leadframe Package
* MicroLeadFrame
* Mini-Cartridge
* Multi-Chip Module
* OPGA
* PQFP
* Package on package
* Pin grid array
* Plastic leaded chip carrier
* QFN
* QFP
* Quadruple in-line package
* ROM cartridge
* Shrink Small-Outline Package
* Single in-line package
* Small-Outline Integrated Circuit
* Staggered Pin Grid Array
* Surface-mount technology
* TO220
* TO3
* TO92
* TQFP
* TSSOP
* Thin small-outline package
* Through-hole technology
* UICC
* Zig-zag in-line package

22 **What is Substrate coupling ?**

Ans In an integrated circuit, a signal can couple from one node to another via the substrate. This phenomenon is referred to as substrate coupling or substrate noise coupling. The push for reduced cost, more compact circuit boards, and added customer features has provided incentives for the inclusion of analog functions on primarily digital MOS integrated circuits (ICs) forming mixed-signal ICs. In these systems, the speed of digital circuits is constantly increasing, chips are becoming more densely packed, interconnect layers are added, and analog resolution is increased. In addition, recent increase in wireless applications and its growing market are introducing a new set of aggressive design goals for realizing mixed-signal systems. Here, the designer integrates radio frequency (RF) analog and base band digital circuitry on a single chip. The goal is to make single-chip radio frequency integrated circuits (RFICs) on silicon, where all the blocks are fabricated on the same chip. One of the advantages of this integration is low power dissipation for portability due to a reduction in the number of

package pins and associated bond wire capacitance. Another reason that an integrated solution offers lower power consumption is that routing high-frequency signals off-chip often requires a 50O impedance match, which can result in higher power dissipation. Other advantages include improved high-frequency performance due to reduced package interconnect parasitics, higher system reliability, smaller package count, smaller package interconnect parasitics, and higher integration of RF components with VLSI-compatible digital circuits. In fact, the single-chip transceiver is now a reality

23 **What is Latchup ?**

Ans A latchup is the inadvertent creation of a low-impedance path between the power supply rails of an electronic component, triggering a parasitic structure, which then acts as a short circuit, disrupting proper functioning of the part and possibly even leading to its destruction due to overcurrent. A power cycle is required to correct this situation. The parasitic structure is usually equivalent to a thyristor (or SCR), a PNPN structure which acts as a PNP and an NPN transistor stacked next to each other. During a latchup when one of the transistors is conducting, the other one begins conducting too. They both keep each other in saturation for as long as the structure is forward-biased and some current flows through it - which usually means until a power-down. The SCR parasitic structure is formed as a part of the totem-pole PMOS and NMOS transistor pair on the output drivers of the gates.

24 **Why is NAND gate preferred over NOR gate for fabrication?**

Ans NAND is a better gate for design than NOR because at the transistor level the mobility of electrons is normally three times that of holes compared to NOR and thus the NAND is a faster gate.

Additionally, the gate-leakage in NAND structures is much lower. If you consider t_phl and t_plh delays you will find that it is more symmetric in case of NAND (the delay profile), but for NOR, one delay is much higher than the other(obviously t_plh is higher since the higher resistance p mos's are in series connection which again increases the resistance).

25 **What is Noise Margin? Explain the procedure to determine Noise Margin**

Ans The minimum amount of noise that can be allowed on the input stage for which the output will not be effected.

26 **What happens to delay if you increase load capacitance?**

Ans delay increases.

27 **What happens to delay if we include a resistance at the output of a CMOS circuit?**

Ans Increases. (RC delay)

28 **What are the limitations in increasing the power supply to reduce delay?**

Ans The delay can be reduced by increasing the power supply but if we do so the heating effect comes because of excessive power, to compensate this we have to increase the die size which is not practical.

29 **How does Resistance of the metal lines vary with increasing thickness and increasing length?**

Ans R = (*l) / A.

30 **For CMOS logic, give the various techniques you know to minimize power consumption?**

Ans Power dissipation=CV2f ,from this minimize the load capacitance, dc voltage and the operating frequency.

31 **What is Charge Sharing? Explain the Charge Sharing problem while sampling data from a Bus?**

Ans In the serially connected NMOS logic the input capacitance of each gate shares the charge with the load capacitance by which the logical levels drastically mismatched than that of the desired once. To eliminate this load capacitance must be very high compared to the input capacitance of the gates (approximately 10 times).

32 **Why do we gradually increase the size of inverters in buffer design? Why not give the output of a circuit to one large inverter?**

Ans Because it can not drive the output load straight away, so we gradually increase the size to get an optimized performance.

33 **What is Latch Up? Explain Latch Up with cross section of a CMOS Inverter. How do you avoid Latch Up?**

Ans Latch-up is a condition in which the parasitic components give rise to the Establishment of low resistance conducting path between VDD and VSS with Disastrous results.

34 **Give the expression for CMOS switching power dissipation?**

Ans CV^2

35 **What is Body Effect?**

Ans In general multiple MOS devices are made on a common substrate. As a result, the substrate voltage of all devices is normally equal. However while connecting the devices serially this may result in an increase in source-to-substrate voltage as we proceed vertically along the series chain (Vsb1=0, Vsb2 0).Which results Vth2>Vth1

36 **Why is the substrate in NMOS connected to Ground and in PMOS to VDD?**

Ans we try to reverse bias not the channel and the substrate but we try to maintain the drain,source junctions reverse biased with respect to the substrate so that we dont loose our current into the substrate.

37 **What is the fundamental difference between a MOSFET and BJT ?**

Ans In MOSFET, current flow is either due to electrons(n-channel MOS) or due to holes(p-channel MOS) - In BJT, we see current due to both the carriers.. electrons and holes. BJT is a current controlled device and MOSFET is a voltage controlled device.

38 **Which transistor has higher gain. BJT or MOS and why?**

Ans BJT has higher gain because it has higher transconductance.This is because the current in BJT is exponentially dependent on input where as in MOSFET it is square law.

39 **Why do we gradually increase the size of inverters in buffer design when trying to drive a high capacitive load? Why not give the output of a circuit to one large inverter?**

Ans We cannot use a big inverter to drive a large output capacitance because, who will drive the big inverter? The signal that has to drive the output cap will now see a larger gate capacitance of the BIG inverter.So this results in slow raise or fall times .A unit inverter can drive approximately an inverter thats 4 times bigger in size. So say we need to drive a cap of 64 unit inverter then we try to keep the sizing like say 1,4,16,64 so that each inverter sees a same ratio of output to input cap. This is the prime reason behind going for progressive sizing.

40 **In CMOS technology, in digital design, why do we design the size of pmos to be higher than the nmos.What determines the size of pmos wrt nmos. Though this is a simple question try to list all the reasons possible?**

Ans In PMOS the carriers are holes whose mobility is less[aprrox half] than the electrons, the carriers in NMOS. That means PMOS is slower than an NMOS. In CMOS technology, nmos helps in pulling down the output to ground ann PMOS helps in pulling up the output to Vdd. If the sizes of PMOS and NMOS are the same, then PMOS takes long time to charge up the output node. If we have a larger PMOS than there will be more carriers to charge the node quickly and overcome the slow nature of PMOS . Basically we do all this to get equal rise and fall times for the output node.

41 **Why PMOS and NMOS are sized equally in a Transmission Gates?**

Ans In Transmission Gate, PMOS and NMOS aid each other rather competing with each other. That's the reason why we need not size them like in CMOS. In CMOS design we have NMOS and PMOS competing which is the reason we try to size them proportional to their mobility.

42 **All of us know how an inverter works. What happens when the PMOS and NMOS are interchanged with one another in an inverter?**

Ans If the source & drain also connected properly...it acts as a buffer. But suppose input is logic 1 O/P will be degraded 1 Similarly degraded 0;

43 **A good question on Layouts. Give 5 important Design techniques you would follow when doing a Layout for Digital Circuits?**

Ans a)In digital design, decide the height of standard cells you want to layout.It depends upon how big your transistors will be.Have reasonable width for VDD and GND metal paths.Maintaining uniform Height for all the cell is very important since this will help you use place route tool easily and also incase you want to do manual connection of all the blocks it saves on lot of area.
b)Use one metal in one direction only, This does not apply for metal 1. Say you are using metal 2 to do horizontal connections, then use metal 3 for vertical connections, metal4 for horizontal, metal 5 vertical etc...
c)Place as many substrate contact as possible in the empty spaces of the layout.
d)Do not use poly over long distances as it has huge resistances unless you have no other choice.
e)Use fingered transistors as and when you feel necessary.

f)Try maintaining symmetry in your design. Try to get the design in BIT Sliced manner.

44 **What is metastability? When/why it will occur?Different ways to avoid this?**

Ans Metastable state: A un-known state in between the two logical known states.This will happen if the O/P cap is not allowed to charge/discharge fully to the required logical levels. One of the cases is: If there is a setup time violation, metastability will occur,To avoid this, a series of FFs is used (normally 2 or 3) which will remove the intermediate states.

45 **Let A and B be two inputs of the NAND gate. Say signal A arrives at the NAND gate later than signal B. To optimize delay of the two series NMOS inputs A and B which one would you place near to the output?**

Ans The late coming signals are to be placed closer to the output node ie A should go to the nmos that is closer to the output.

46 **What is Setup ?**

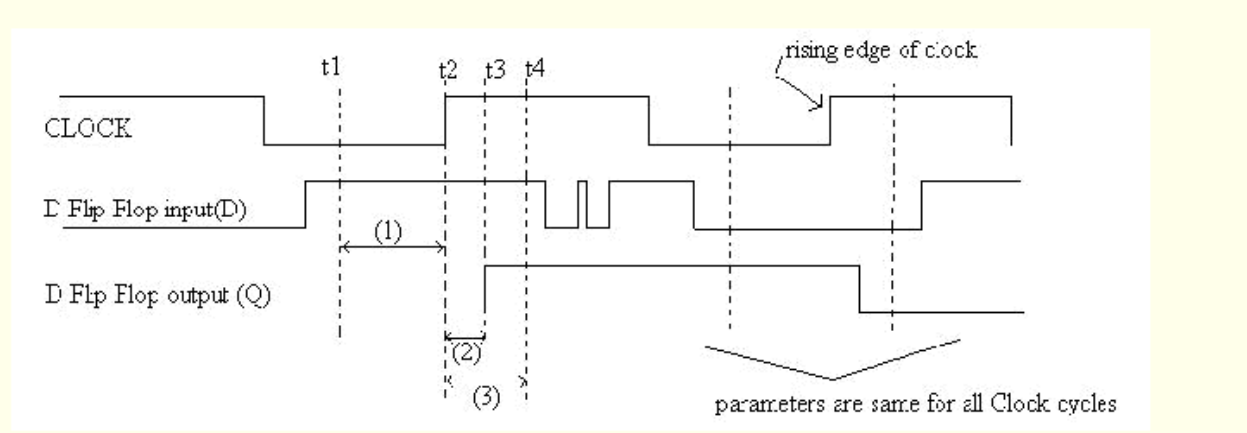
Ans *Setup time is a timing parameter associated with Sequential Devices (for simplicity henceforth I will be only referring to the Flip Flop). The Setup time is used to meet the minimum pulse width requirement for the first (Master) latch makes up a flip flop is. More simply, the setup time is the amount of time that an input signal (to the device) must be stable (unchanging) before the clock ticks in order to guarantee minimum pulse width and thus avoid possible metastability.*

47 **What is Hold time?**

Ans *Hold time is also a timing parameter associated with Flip Flops and all other sequential devices. The Hold time is used to further satisfy the minimum pulse width requirement for the first (Master) latch that makes up a flip flop. The input must not change until enough time has passed after the clock tick to guarantee the master latch is fully disabled. More simply, hold time is the amount of time that an input signal (to a sequential device) must be stable (unchanging) after the clock tick in order to guarantee minimum pulse width and thus avoid possible metastability.*

48 **What is a timing diagram? Can we use it to better understand Setup and Hold time?**

Ans *Timing diagram is a complete description of a digital machine. We can use the timing diagram (waveform) to illustrate Setup and Hold time. Observe the waveform given below:*



From the timing diagram we observe that we have three signals: the Clock, the Flip Flop Input (D) and the Flip Flop output (Q). We have four timing instances and three time periods. The inferences from this waveform will help us understand the concept of propagation delay Setup and Hold time.

(1) i.e. [t2 - t1] is the Setup Time: the minimum amount of time Input must be held constant BEFORE the clock tick. Note that D is actually held constant for somewhat longer than the minimum amount. The extra "constant" time is sometimes called the setup margin.

(2) i.e. [t3 - t2] is the Propagation delay of the Flip Flop: the minimum/maximum time for the input to propagate and influence the output.

(3) i.e. [t4 - t2] is the Hold time: the minimum amount of time the Input is held constant AFTER the clock tick. Note that Q is actually held constant for somewhat longer than the minimum amount. The extra "constant" time is sometimes called the hold margin.

(The above timing diagram has 2 clock cycles; the timing parameters for the second cycle will also be similar to that of the first cycle)

49 **What timing parameters are commonly used?**

Ans *The list of the timing parameters that you may be asked to calculate for a given sequential circuit is*

1. *Propagation delay, Clock to Output (minimum)*
2. *Propagation delay, Clock to Output (maximum)*
3. *Propagation delay, Input to Output (minimum)*

4. *Propagation delay, Input to Output (maximum)*

5. *Setup Time (Data input before clock)*

6. *Hold Time (Data input after clock)*

7. *Maximum Clock rate (or its reciprocal, minimum clock period)*

50 **How do we find the Propagation delay, Clock to Output?**

Ans *Propagation delay (PD) for the circuit can be calculated as the summation of all delays encountered from where the clock occurs to the output. In short, the delays of the State memory and the output logic.*

$PD_{Clock\text{-}Output}(min) = R_{pd\ (min)} + G_{pd\ (min)}$

$PD_{Clock\text{-}Output}(max) = R_{pd\ (max)} + G_{pd\ (max)}$

51 **How do we find the Propagation delay, Input to Output?**

Ans *This is a property associated with Mealy machines only. In other words, for a Moore machine the value for this timing parameter is infinity (∞). The calculation (for mealy machines) is the summation of all propagation delays encountered between the input (that influences the output by bypassing the state memory) and the output.*

For MOORE machines:

$PD_{Input\text{-}Output}(min) = infinity\ (\infty)$

$PD_{Input\text{-}Output}(max) = infinity\ (\infty)$

For MEALY Machines

$PD_{Input\text{-}Output}(min) = G_{pd\ (min)}$

$PD_{Input\text{-}Output}(max) = G_{pd\ (max)}$

52 **How do we calculate Setup time?**

Ans The calculation for setup time is the sum of the setup time for the concerned flip flop and the maximum delay from the input logic.

$T_{SETUP} = R_{SETUP} + F_{pd\,(MAX)}$

53 **How do we get the value for the Hold time?**

Ans The value for the Hold time can be obtained by the following formulae

$T_{HOLD} = R_{HOLD} - F_{pd\,(MIN)}$

The concern here is how soon (minimum time) an erroneous input can propagate in from the Input logic while the Flip Flop is attempting to hold on to a stable value. The negative sign can be associated with 'after the clock occurs' to ease in remembering this formulae.

54 **How do we calculate the Maximum Clock rate (MCLK)?**

Ans Maximum clock rate is calculated using the formula

$MCLK = 1/ T_{MIN}$

So we will have to calculate T_{MIN} first. T_{MIN} here refers to the minimum time period for correct operation of the circuit, so it is calculated using all worst cases (maximum delays).

$T_{MIN} = F_{pd\,(MAX)} + R_{SETUP} + R_{pd\,(MAX)}$

So having found the minimum clock period let us now calculate for the MCLK

$MCLK = 1/ T_{MIN} = (Fpd_{(MAX)} + R_{SETUP} + R_{pd\,(MAX)})^{-1}$

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